taifatech inc.
泰發科技股份有限公司

TF-900

Datasheet Brief

Revision History

Revision	Date	Descriptions
V1.0	2014-10-21	First release
V1.1	2015-08-20	Update

Introduction

Overview

TF-900 integrates Quad-Core 64-bit Cortex-A53 CPU with advanced SIMD co-processor and VFPv4 instruction set. It is latest 28nm super high performance Application Processor with low power consumption. The compact integrated PowerVR G6230 GPU and Video Processing Unit provides perfect H.265 4K video effects and gaming experience. The advanced ISP supports camera sensors up to 13M pixel resolutions.

TF-900 provides rich interfaces such as HDMI, eDP, MIPI CSI, DSI, LVDS and USB3, etc. Bluetooth, WiFi and display peripherals can be easily integrated to construct flexible solutions. Efficient memory systems are built on high performance DDR3/DDR3L/LPDDR2/LPDDR3 and large capacity dual channel NAND Flash controller.

Together with companion chip ATC260x which integrated PMU and Audio Codec together, TF-900 makes it the best choice for high performance open platform.

Applications of TF-900 include but not limited to the followings:

- Ultra book
- Smart Video Monitors
- Action Cameras
- Tablet
- MID (Multimedia Internet Device)
- POS machines
- Advertising Machines
- Other Cloud-connected applications

Features

Central Processing Unit (CPU)

- Quad-core 64-bit ARM Cortex-A53 processor, up to 1.6GHz
- Individualized power domain per core
- 32KB Icache and 32KB Dcache per core
- 1MB L2 cache
- ARMv8-A Architecture:
  - Double Precision Floating Point SIMD, allows SIMD vectorization to be applied to a much wider set of algorithms
  - 64-bit Virtual address reach, Enables virtual memory beyond 4GB.
  - Larger register files, 31 x 64b general purpose registers: increases performance, reduces stack use.
  - Efficient 64-bit immediate generation, less need for literal pools
  - Large PC-relative addressing range,+/-4GB
  - Tagged Pointers, useful for dynamically typed languages such as JavaScript, and for garbage collection
  - 64k pages, reduce TLB miss rates and depth of page walks

- New exception model, reduces OS and Hypervisor software complexity
- Enhanced Cache management, user space cache operations improve dynamic code generation efficiency

- Advanced Floating point and SIMD technology accelerates the performance of multimedia applications
- Full CoreSight debug supported
- Secure RW supported, including TrustZone
- Multi-voltage domain, support DVFS

Graphics Processing Unit (GPU)

- Imagination PowerVR G6230 GPU
- OpenGL-ES1.1/2.0/3.0/3.1, OpenGL 3.2, DirectX 10, OpenCL 1.2EP
- Rasterisation
  - Deferred Pixel Shading
  - On-chip tile floating point depth buffer
  - 8-bit stencil with on-chip tile stencil buffer
  - 32 parallel depth/stencil tests per clock
  - Scissor test (up to 16K scissor rectangles supported)
- Texture parameters
  - Up to 16K * 16K textures (IMG Hardware decode support 16k*16k, software decode support 8k*8k)
  - Volume textures (2K depth)
  - Stride textures up to 32K size for the stride
  - Full arbitrary non power of two texture support
  - Constrained non power of two stride based textures
  - 1 TB virtual address range
- Address modes
  - All DirectX 10, OpenGL 3.2, and OpenGL ES 3 texture addressing modes
- Texture lookups
  - Un-normalised/integer 1D and 2D texture coordinates (up to 64K * 64K)
  - Multi-sample texture addressing (up to 8 samples per texel)
  - Imagination Technologies Strictly Confidential
  - Sample offsets in the range [-31,+32] for 1D, 2D and 3D textures together with multi-sample textures
  - Not-normalized texture lookups
  - Integer lookups
  - Fetch N support
  - Gather 4 support
  - Load instruction support
  - Texture writes enabled through the Texture Processing Unit

- Filtering
  - Sample details: sample data and coefficient support
  - Bilinear, Trilinear and Anisotropic filtering

- Bi-cubic filtering of 8-bit surfaces
- Corner filtering support for Cube Environment Mapped textures and filtering across faces

- Texture formats
  - All OpenGL ES 3, OpenGL 3.2 and DirectX 101 texture formats
  - PVRTC I & II
  - Frame buffer compression formats (not in all variants)
  - YUV planar support with arbitrary allocation for the planes and up to 16 different configurable coefficients and chroma interpolation
- Gamma support
  - Pre-multiplied Alpha
  - Gamma corrected textures on unsigned 8-bit RGB (A) and XR textures
- Mipmapping support
  - Fractional top and bottom LOD clamps (minimum LOD and maximum LOD)
  - Number of mipmap levels present for a given texture and fractional minimum level
- Renderable formats
  - All OpenGL ES 3.2, OpenGL ES 3 and DirectX 101 output formats
- Resolution Supported
  - Frame buffer max size = 16K * 16K
  - Texture max size = 16K * 16K
- Anti-aliasing
  - 2x, 4x, 8x Multisampling
- Primitive Assembly
  - Bus mastered
  - Programmable vertex DMA
  - Indexed and non-indexed primitive lists
  - Point, line, line strip, line loop, triangle list, triangle fan, triangle strip, and patch primitives with adjacency
  - 8-bit, 16-bit and 32-bit indices
  - 256-entry post shader vertex cache
  - Early hidden object removal
  - Vertex compression
  - Tile acceleration
- Render to texture
  - Twiddled format support
  - Multiple on-chip render targets (MRT) 2
  - Lossless Frame Buffer Compression (and Decompression) (Not in all variants)
  - Programmable Geometry Shader Support
  - Direct Geometry Stream Out (Transform Feedback)

- Unified Shader

- Four ALU pipelines per USC
- Each ALU pipeline operates on 16 simultaneous instances for high utilization
- 512 concurrent data instances
- Unified 4 banks by 128 bit x 1024 deep common store (Shader Constants and Triangle Coefficients)
- Local data, texture and instruction caches (L0 cache)
- Variable length instruction set encoding
- Full support for OpenCL™ atomic operations (except compare exchange)
- Scalar and vector SIMD execution model
- Alpha to Coverage

Video Decoder

- Video format and performance
  - MPEG-4 XviD/DivX (3.11/4.x/5.x/6.0) SP/ASP@L5/GMC 1080p@60fps
  - H.263 Profile0/3 (Sorenson H.263) 1080p@60fps
  - H.264 (x264) /MPEG4 AVC BP/MP/HP/MVC extension, up to 4k*2k
  - AVS, 1080p@60fps,
  - AVS+, VP9, WMV7/8 supported
  - VP6 (VP6.0/VP6.1/VP6.2), VP8 (webP/webM), 1080p@60fps
  - WMV9/VC-1 SP/MP frame mode 1080p@60fps
  - RM 1080p@60fps
  - MEPG-2 MP@ML 1080p@30fps and 1080i@60fps supported
  - MPEG-1 1080p@60fps
  - 60Mbps average bit rate and 120Mbps peak bit rate2D-cache for saving bandwidth
- JPEG format and performance
  - YUV400, YUV420, YUV211H, YUV211V, YUV422, YUV444
  - JPEG baseline 48*48 up to 30000*30000
  - JPEG progressive 48*48 up to 8176*8176
- Post processing (only for H.264)
  - 90 angle rotation
  - 1/2 horizontal and/or vertical down sample
  - Post processing output stride is programmable

HEVC Decoder

- Video format and performance
  - HEVC/H.265 Main/Main10/Main Still Picture profiles
  - 4096*2304 @30fps
  - Support 10-bit bit stream decoding
- Post processing
  - 90 angle rotation
  - 1/2 horizontal and/or vertical down sample
  - Post processing output stride is programmable

Video Encoder

- Pre-processor
  - YCbCr411, 420/YCrCb411, 420 (planner or semi-planner), ARGB32 (variances), RGB565
  - 1/2 to 8 scale, bilinear scaling
- Video format and performance
  - H.264 baseline profile, up to 1920*1088@60fps
  - I/P slice
  - 1/4 Pixel motion compensation
  - Context-based Adaptive Variable Length Coding (CAVLC) .
  - Bitrate control (CBR/VBR)
  - Ts remuxer supported
  - Ultra low delay encoding for low latency application (Miracast), MVC supported
- JPEG format and performance
  - JPEG baseline, up to 8176*8176
  - Support concurrent Photo taking while recording
  - Huffman/quant configurable table

Video IN

- Camera Interface & Image Signal Processor
  - 2 channel input (4lanes MIPICSI,2lanes MIPICSI or DVP)
  - Dual cameras simultaneously, support 3D input, PIP (Picture In Picture)
  - Input Format: Bayer RAW, YUV422, YUV420
  - High accuracy processing (12-bit pipeline)
  - 2 pixels/Clk processing
  - Maximum input resolution 8192*4096
  - Input Windowing and Scale
  - Fast capture
  - Auto detect Black level and compensation
  - Four channel Color Lens shading correction
  - 3A (Auto Focus, Auto White Balance, Auto Exposure)
  - Defect pixel correction
  - Bayer Noise Reduction
  - Bayer Demosaicing
  - Color Space Conversion
  - Color correction matrix
  - False Color Suspension
  - Chrome Color Suspension
  - Backlighting Compensation
  - R/G/B Gain Adjustment
  - R/G/B Gamma Correction
  - Histogram Information
  - AWB/AE/AF statistics for 3A

- White pixel detection and Color temperature estimation
- Contrast, Saturation, Hue, Brightness Adjustment
- Support color fixed for effect
- Chrome Down Sample
- Support RAW data capture

- Image Enhance Processor
  - Support 9x9, 7x7, 5x5, 3x3 filter for image Noise Reduction
  - Adaptive Edge Enhancement (Laplace filter)
  - Support size from 128*128 to 8192*8192
  - YUV420 semi-planar and YUV420 planar
  - Up to 1080p@60fps

Display Subsystem

Display Engine

- Four video layer
  - 24bit programmable background layer
  - ARGB8888, ARGB1555, RGB565 and these variance, up to 2560*2048
  - YUV420 semi-planner & YUV420 planner, up to 4096*2304
  - 1/4 to 8 hi-quality scalar in horizontal & vertical
  - hi-quality scalar (lanczos/bicubic/bilinear mode)
  - Brightness, contrast and saturation adjustment
  - Flip in horizontal and vertical
- Two blender
  - Up to 4 layer alpha-blending (coverage/pre-multiply mode) .
  - Global or per-pixel alpha.
- Others
  - VC1 remapping
  - 3D HDMI display
  - Key registers double buffer
  - Gamma Correction
  - Dither (FRC mode) after gamma
  - Two output path simultaneously, LCD & HDMI
  - Embedded memory management unit (MMU)
  - Histogram statics for Y samples (32 steps) for LCD path only
  - Two AXI port and dynamic QoS control

HDMI/MHL

- Support HDMI 1.4b & MHL 2.1
- For HDMI 1.4b Supports for the following:
  - Up to 1080p@60 & 4K*2K@30fps
  - 3D video mode

- Up to 12bit Deep Color
- HPD Detect
- HDCP 1.4

- For MHL2.1 Supports for the following:
  - 24bit RGB and YCbCr4:4:4, up to 720P@60fps
  - Packed Pixel YCbCr4:2:2 format, up to 1080p@60fps

LVDS

- Support dual channel LVDS interface LCD
- Support max clock frequency up to 200M
- Support LVDS RGB 24/18bit data
- Support data lanes swap for convenient PCB design

MIPI DSI

- Compliant with MIPI DSI Specification version 1.1 and the D-PHY specification version 1.1
- 1-4 data lanes, from 75 Mbps to 1Gbps per lane
- Support Command and Video mode Transmissions
- Pixel Format:
  - Command Mode: 8bits, 12bits, 16bits, 18bits, and 24bits per pixel
  - Video Mode: RGB565, RGB666 (Packed), RGB666, and RGB888
- Support data lanes swap for convenient PCB design

eDP

- Compliant with eDP specification V1.3
- 1/2/4 data lanes
- 1.62Gbps, 2.7Gbps, 5.4Gbps
- Support Aux channel
- Support panel self refresh (PSR)
- Support data lanes swap for convenient PCB design

Internal Memory

Boot ROM

- Size: 64KB
- Support boot device:
  - eMMC
  - NAND Flash (Async/Toggle/DDR)
  - SD/MMC
  - SPI NOR
- USB driver is inside for upgrading firmware and hardware test
- Sign check for secure OS firmware

Share SRAM

- Secure access only: 32KB
- Secure or non-secure access: 96KB

External off-chip Memory

DRAM

- Compatible with JEDEC standard DDR3/DDR3L/LPDDR2/LPDDR3, frequency up to 720MHz
- Support 2 channel, each channel data width can be 32-bit or 16bit, which is
- software-configurable
- Support 2 ranks (chip selects) for each channel
- Up to 4GB address space
- Support hardware auto calibration & dynamic drift compensation function
- Advanced command reordering and scheduling to maximize bus utilization
- Support JEDEC Standard Low-power Mode

NAND Flash

- Support Dual Channel NAND controller, each channel 8bits
- Up to 70-bit BCH ECC
- Async & Sync Mode support, Max Speed Up to DDR200
- SLC, MLC & TLC NAND & Managed NAND Flash support
- Support Dual EMMC & NAND Flash

SD/ MMC/EMMC

- Four SD/ MMC/EMMC controller
- Support SD3.0 and MMC4.5 protocol
- Support eMMC4.5
- Clock max to 200MHz
- Support boot mode based on eMMC4.5 SPEC.
- Integrated Clock Delay Chain Technique to Regulate Card Interface Timing.
- Build-in pull up resistance for CMD/DAT lines.

System Control

Clock management unit

- One oscillator with 24Mhz clock input and embedded 10 PLLs
- Support SSC function for special PLL, such as FLASH.

Speed and Temperature Sensor

- Speed sensor give module max speed
- Temperature sensor accuracy, +-5 degree

Timer

- Four timers running at fixed 24MHz
- Two timers only secure accessible

Secure Control and Accelerator

- ARMR TrustZoneR Security
- Secure SRAM is included for security service
- Secure accelerator for AES-128 Encrypt & Decrypt in ECB/CBC/CBC-CTS/CTR mode
- Support One-Time Programmable root key
- Key management in security system

- Built-in HDPC 2.2 hardware support
- Secure data path control
- Support Secure Boot

High speed peripherals

USB3

- Compliant with USB3.0 Specification
- Support USB Supper Speed (5Gb/s), High Speed (480Mb/s) and Full Speed (12Mb/s) in
- device mode
- Support USB Supper Speed, High Speed ,Full Speed and Low Speed (1.5Mbp/S) in host mode
- Support HUB
- Support USB Remote wakeup function

USB2

- Two USB OTG 2.0 Controller
- Compliant with USB OTG 2.0 Specification
- Support High Speed ,Full Speed and Low Speed
- Supports HUB
- Support HSIC Interface
- Support 15 IN endpoints and 15 OUT endpoints besides Control endpoint0
- Support remote wakeup function

More Interfaces

- Support 10/100M Ethernet MAC with RMII/SMII interface
- Six TWI (Two Wire Interface) Controller Integrated, Max speed up to 3.4Mbps (High Speed mode)
- Seven UART Controller Integrated, Max speed up to 3Mbps
- IRC Controller integrated, Support RC5/RC6/NEC/9012 Protocol
- Four SPI Controller Integrated
- Support six programmable PWM Output
- Support I2S, PCM and SPDIF audio interface

Power Management

- Multiple Power Domains and automatic Power Status tracking
- Internal Dynamic power adjustment supported
- Internal Dynamic clock adjustment supported
- Multiple standby status supported
- New Generation Ultra Low Power Design (“ULPD”)

Package

- FCCSP642, 19mm*19mm, 0.65mm Pitch

Application Diagram

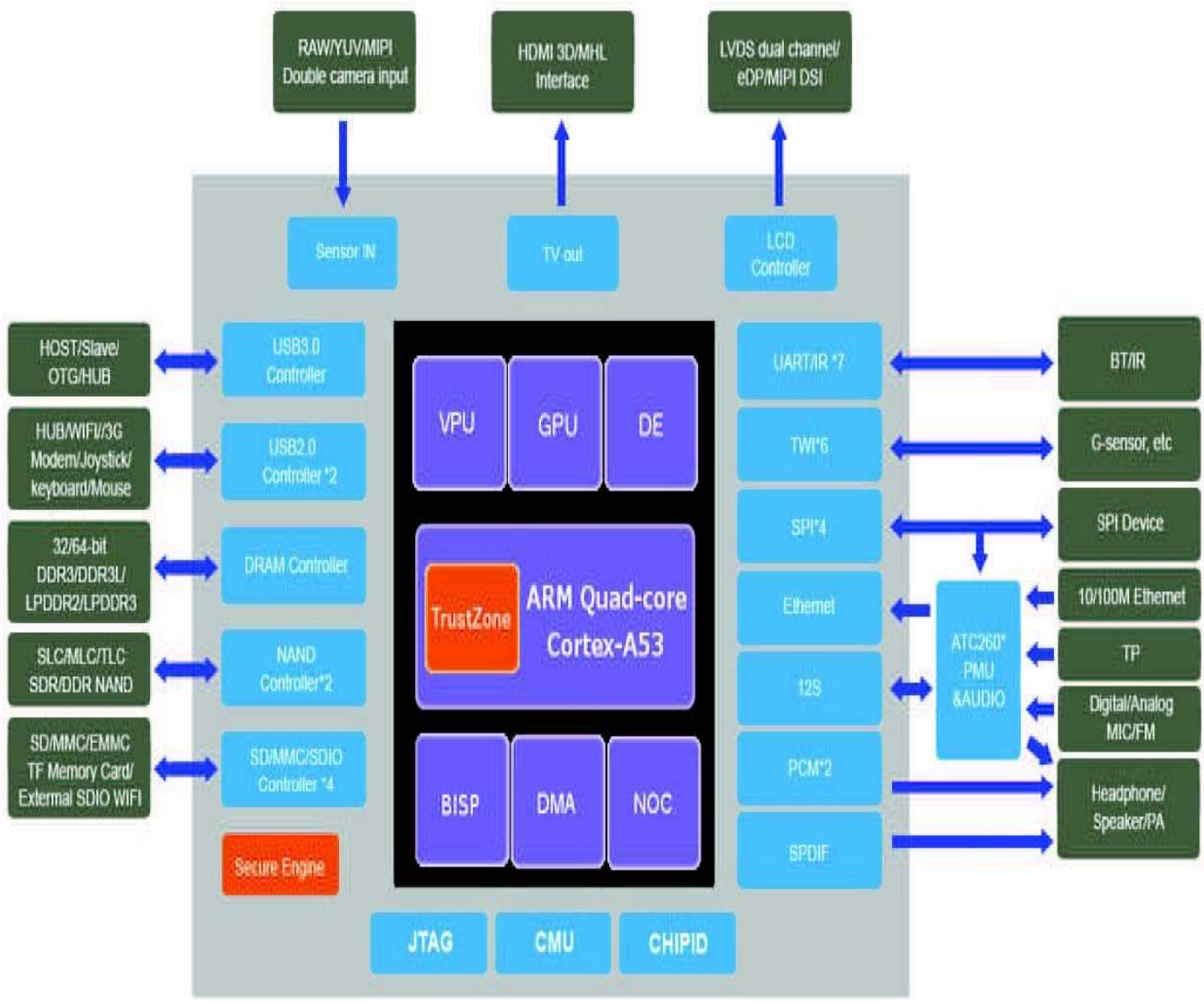

Figure 1-1 TF-900 Application Diagram